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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/398,652	09/17/1999	WILLIAM A. SAMARAS	042390.P5120D	1359

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EXAMINER
CHANG, RICK KILTAE

ART UNIT	PAPER NUMBER
3729	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/398,652	Applicant(s) SAMARAS ET AL.	
	Examiner Rick K. Chang	Art Unit 3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19 and 21-26* is/are pending in the application.

4a) Of the above claim(s) *22 and 24-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19,21,23 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 19, 21, 23 and 26 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for coupling solder balls to the interposer, does not reasonably provide enablement for "soldering a plurality of cache memory devices and at least one passive device to the first surface" (claim 19, lines 6-7), "soldering said interposer to a substrate" (claim 19, line 11), and "soldering a microprocessor device to the substrate" (claim 19, line 13). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. The specification is silent as to how the electronic devices are coupled to each other.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 19, 21, 23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seidel (US 5,635,847) in view of Gedney et al (US 5,483,421), and further in view of Beers (US 5,680,936).

Re claim 19: Seidel discloses providing an interposer (10); coupling solder balls (12) to the interposer (10); coupling a plurality of semiconductor dice (11) to the first surface (the

surface where 11s are mounted); and testing the plurality of semiconductor dice (11) on the interposer (col. 1, lines 20-34 and col. 2, lines 46-51).

Seidel fails to disclose populating the second surface with a plurality of conductive pads; coupling the solder ball to each of selected ones of the plurality of conductive pads; coupling at least one passive device to the first surface; coupling the interposer to a substrate with the solder balls after the testing if the plurality of semiconductor dice pass the testing; coupling at least one other semiconductor device to the substrate; soldering a plurality of cache memory devices and at least one passive device to the first surface; soldering said interposer to a substrate; and soldering a microprocessor device to the substrate.

Gedney discloses populating the second surface with a plurality of conductive pads (32); coupling a solder ball (44) to each of selected ones of the plurality of conductive pads (32); soldering (col. 8, lines 1-7) the interposer (24) to a substrate (38) with the solder balls (44); and soldering (col. 7, lines 47-56) at least one other semiconductor device (Fig. 4 shows a third semiconductor device (20 and 24) is mounted on 38) to the substrate (38) thereby forming a multi-chip subassembly and mounting this subassembly to printed circuit cards (col. 1, lines 7-8) without any defective components.

Beers discloses soldering at least one passive device (see annotated Fig. 3 below and col. 1, lines 28-32) thereby regulating voltage and current to the electronic dice.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Seidel by populating the second surface with a plurality of conductive pads; coupling a solder ball to each of selected ones of the plurality of conductive pads; soldering the interposer to a substrate with the solder balls; and soldering at least one other semiconductor

device to the substrate, as taught by Gedney, for the purpose of forming a multi-chip subassembly and mounting this subassembly to printed circuit cards without any defective components.

Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Seidel by coupling at least one passive device to the first surface of the interposer, as taught by Beers, for the purpose of regulating voltage and current to the electronic chip.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to incorporate a plurality of cache memory devices and a microprocessor device to use in a computer to perform computation and temporarily store program applications.

Therefore, it would have been an obvious matter of design choice to modify Seidel to obtain the invention as specified in claim 19.

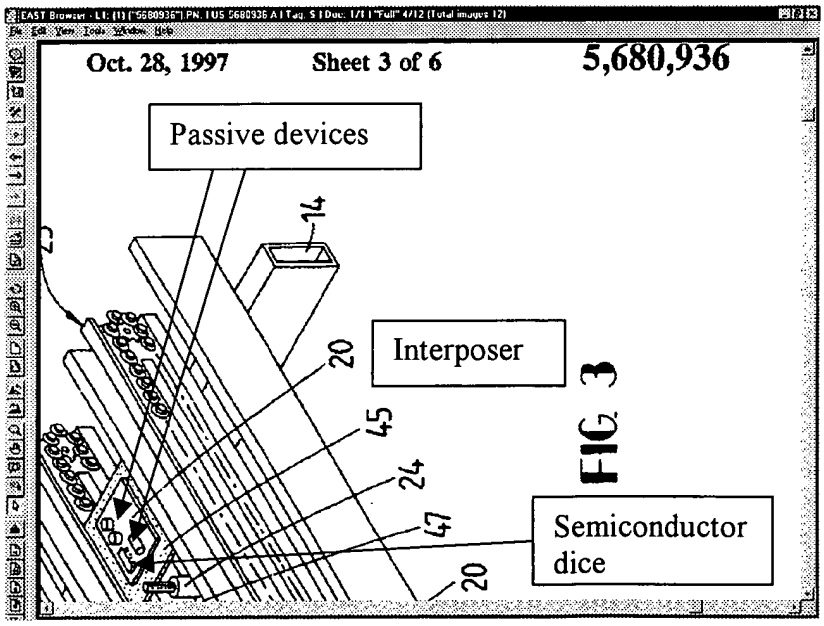

FIG 3

Re claim 21: Seidel teaches the invention as described with respect to claim 19 above.

Seidel fails to disclose providing the interposer having organic material.

Gedney discloses providing the interposer (24) having organic material (col. 7, lines 15-16) thereby providing low thermal coefficient of expansion.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Seidel by providing the interposer having organic material, as taught by Gedney, for the purpose of providing low thermal coefficient of expansion.

Re claim 23: Seidel teaches the invention as described with respect to claim 19 above. Seidel discloses scrapping the semiconductor dice coupled to the interposer without any further work if the plurality of semiconductor dice does not pass the testing (col. 1, lines 20-34).

Re claim 26: Seidel teaches the invention as described with respect to claim 19 above.

Seidel fails to disclose creating a plurality of contacts on the substrate; and electrically connecting the selected ones of the plurality of conductive pads to the plurality of contacts.

Gedney discloses creating a plurality of contacts (42) on the substrate (38); and electrically connecting the selected ones of the plurality of conductive pads to the plurality of contacts (Fig. 5 shows conductive pads 32 are electrically connected to the contacts 42 via solder balls 44) thereby allowing signal to travel from one part of the component to another and providing power and ground to the device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Seidel by creating a plurality of contacts on the substrate; and electrically connecting the selected ones of the plurality of conductive pads to the plurality of contacts, as taught by Gedney, for the purpose of allowing signal to travel from one part of the component to another and providing power and ground to the device.

Response to Arguments

4. Applicant's arguments filed March 12, 2002 have been fully considered but they are not persuasive.

The specification does not reasonably provide enablement for the limitations "soldering a plurality of cache memory devices and at least one passive device to the first surface" (claim 19, lines 6-7), "soldering said interposer to a substrate" (claim 19, line 11), and "soldering a microprocessor device to the substrate".

However, Gedney discloses soldering (col. 8, lines 1-7) the interposer (24) to a substrate (38) with the solder balls (44); and soldering (col. 7, lines 47-56) at least one other semiconductor device (Fig. 4 shows a third semiconductor device (20 and 24) is mounted on 38) to the substrate (38). Beers discloses soldering at least one passive device (col. 1, lines 28-32).

Conclusion

5. Applicants are duly reminded that a full and proper response to this Office Action that includes any amendment to the claims and specification of the application as originally filed requires that the applicant point out the support for any amendment made to the disclosure, including the claims. See 37 CFR 1.111 and MPEP 2163.06.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rick K. Chang whose telephone number is (703) 308-4784. The examiner can normally be reached on 5:30 AM to 1:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter D. Vo can be reached on (703) 308-1789. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9302 for regular communications and (703) 872-9303 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1148.

Rick K. Chang
Examiner
Art Unit 3729

RC
March 15, 2002